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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AKIHIKO KOH, TSUTOMU SAMPEI,
NOBUHISA WATANABE, and AKIHIRO KIKUCHI

Appeal 2009-004407
Application 09/802,857
Technology Center 2100

Decided: May 14, 2010

Before JAMES D. THOMAS, JOSEPH F. RUGGIERO, and
MAHSHID D. SAADAT, *Administrative Patent Judges*.

THOMAS, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 27, 28, 40, and 45 through 52. We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing was conducted on this appeal on May 6, 2010.

We reverse and institute a new ground of rejection within the provisions of 37 C.F.R. § 41.50(b).

Invention

The present invention relates to a data processing apparatus including at least a central processing unit and a memory providing programs for the CPU, which is able to correct bugs in the programs stored in the memory after manufacture. (Spec. 1, ll. 5-10.)

Prosecution History

The record in this application reveals that a prior Decision was mailed on October 31, 2006, denominated as Appeal No. 2006-2407, in which we affirmed the Examiner's rejection of all the claims then on appeal under 35 U.S.C. § 103. This application was also subject to a Request for Rehearing in this latter noted appeal, a decision which was mailed on June 21, 2007, where we decided to not make any changes to our prior Decision.

Representative Claim

27. A data processing apparatus comprising:

a bug address setting register adapted to store a bug address, said bug address indicating an address for a buggy data;

a coincidence detecting circuit adapted to compare said address with said bug address and output an interrupt request signal, said interrupt request signal indicating coincidence or non-coincidence of said address and said bug address;

a central processing unit adapted to process an interrupt function upon receipt of said interrupt request signal; and

a counter register adapted to store a value, said value representing a number of times said interrupt request signal indicates a coincidence between said address and said bug address.

Prior Art and Examiner's Rejections

The Examiner relies on the following references as evidence of unpatentability:

Sagane	5,454,100	Sep. 26, 1995
Hosotani	5,701,506	Dec. 23, 1997
Suzuki	5,784,537	Jul. 21, 1998
Koscal	6,412,081 B1	Jun. 25, 2002 (filed Jan. 15, 1999)

Claims 45 through 52 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite since independent claim 45 does not have antecedent basis for the feature within the wherein clause reciting "said initialization processing." Additionally, all claims on appeal, claims 27, 28, 40, and 45 through 52, stand rejected under 35 U.S.C. § 103. As to claims 27, 28, and 40, the Examiner relies upon Sagane in view of Suzuki in a first stated rejection. Next, the Examiner relies upon this combination of references, further in view of Koscal, as to claims 45 through 50. Lastly, in a third stated rejection, as to claims 51 and 52, the Examiner relies upon Sagane in view of Suzuki and Koscal, further in view of Hosotani.

ANALYSIS

For the reasons set forth subsequently in this opinion, with respect to all claims on appeal, claims 27, 28, 40, and 45 through 52, the existing prior art rejections must be reversed *pro forma* because they are necessarily based on speculative assumptions and inferences as to the meaning of the claims. *See In re Steele*, 305 F.2d 859, 862-863 (CCPA 1962). It should be understood, however, that our decision in this regard is based solely on the indefiniteness of the claimed subject matter and does not reflect the adequacy or the inadequacy of the prior art evidence applied in support of the rejection before us. Once definite claims are presented, the Examiner is free to apply the same, different, or additional prior art if the Examiner so chooses.

New Rejection within 37 C.F.R. § 41.50(b)

Claims 27, 28, 40, and 45 through 52 are rejected under the second paragraph 35 U.S.C. § 112 as being indefinite.

As to independent claim 27, the scope of meaning to be attributed to the term "a buggy data" is not reasonably determinable. The functionality of the coincidence circuit is to perform a compare functionality, but the result of the statement of that compare operation is not stated such as to indicate that a coincidence is detected when the same or different addresses are present. Moreover, in this regard, it is not clear what the term "said address" refers back to. The only recitation of an address is "a bug address." Yet, a compare function would also be indeterminable since the compare function may be interpreted, as recited, to compare a bug address with a bug address

which appears to be indefinite on its face. The conditions under which or when an output of an interrupt request signal would be indicated is not established by the actual recitations in claim 27. Indeed, the interrupt request signal is recited to indicate a coincidence or non-coincidence of "said address" with the bug address, which recitations are inclusive of the problems already identified as well as a lack of a definite statement as to whether the interrupt request signal indicates either a coincidence or a non-coincidence of address signals or, as recited, ambiguously both.

As to independent claim 40, the wherein clause at the end of the claim, reciting "wherein said value of the counter register is incremented by 1," does not appear to follow from the previous recitations either in a logical or functional sense. The claim remains indefinite as to under what conditions or why such an incrementing function would occur. Ambiguities also exist since there is an absence of the generation of an interrupt request signal. The initial wherein clause, reciting another program address indicating a location within a program memory, does not appear to have any functional significance according to the recitations among the other recited parts of this claim as a whole. This claim appears functionally incomplete.

Lastly, we turn to independent claim 45. This claim has several recitations of first and second as applied to interrupt request signals, coincidence detecting circuits, bug addresses, and the like among several interrelated clauses. The claim fails to specify that the first and second recitations in the various clauses are with respect to different entities or elements. The first and second recitations may apply to a single given circuit element at different points in time. These ambiguities alone appear to

cause the claim to be read in different degrees of scope and in different manners. The claim also does not recite, as the Examiner aptly indicates in the Examiner's own rejection under § 112 second paragraph, the actual recitation of an initialization processing to which the last clause, the wherein clause, refers when it states "said initialization processing."

CONCLUSION AND DECISION

We have *pro forma* reversed the three outstanding rejections under 35 U.S.C. § 103 that encompass all claims on appeal, claims 27, 28, 40, and 45 through 52. We maintain and adopt as our own the Examiner's views with respect to the Examiner's own rejection of claims 45 through 52 under the second paragraph of 35 U.S.C. § 112. On this same statutory basis, we have instituted our own rejection of all claims on appeal.

This decision contains new grounds of rejection pursuant to 37 C.F.R. § 41.50(b). Section 41.50(b) provides that "[a] new ground of rejection . . . shall not be considered final for judicial review."

Section 41.50(b) also provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .

(2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

REVERSED
37 C.F.R. § 41.50(b)

msc

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